

AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

Claim 1 (Cancelled)

2. (Currently Amended) A method of synthesizing a register transfer level (RTL) based design of a system comprising the steps of:

determining a plurality of sub-modules of a top level system;

determining individual time budgets for each sub-module based on timing requirements of the top-level system;

synthesizing a gate-level design of ~~the sub-modules~~ said each sub-module based on the determined time budgets for ~~the individual sub-modules~~ said each sub-module;

testing the gate-level ~~designs~~ design of said each sub-module for conformance with ~~gate-level design requirements of the individual sub-modules~~ said each sub-module;

generating a netlist for said each sub-module when the gate level design of said each sub-module conforms to said design requirements of said each sub-module, then integrating the ~~gate-level designs~~ netlist of the individual sub-modules said each sub-module to form a an integrated top level design netlist;

testing the integrated top-level design netlist for conformance with top-level design requirements; and

generating a top-level netlist when the integrated top-level design netlist conforms to the top-level design requirements; and

~~generating gate-level netlists for the gate-level designs of each of the sub-modules.~~

Claims 3 - 4 (Cancelled)

5. (Currently Amended) A method of synthesizing a register transfer level (RTL) based design of a system comprising the steps of:

determining a plurality of sub-modules of a top level system;

determining individual time budgets for each sub-module based on timing requirements of the top-level system;

synthesizing ~~gate-level designs~~ a gate level design of the ~~sub-modules~~ said each sub-module based on the determined time budgets for ~~the individual sub-modules~~ said each sub-module;

testing the ~~gate-level designs~~ gate level design of said each sub-module for conformance with ~~gate-level~~ design requirements of ~~the individual sub-modules~~ said each sub-module;

generating a netlist for said each sub-module when the gate level design of said each sub-module conforms to said design requirements of said each sub-module, then integrating the ~~gate-level designs~~ netlist of the ~~individual sub-modules~~ said each sub-module to form a an integrated top level design netlist;

testing the integrated top-level design netlist for conformance with top-level design requirements; and

generating a top-level netlist when the integrated top-level design netlist conforms to the top-level design requirements,

wherein testing the ~~gate-level~~ gate level design ~~netlist~~ include of said each sub-module includes performing static timing analysis on ~~the individual sub-modules~~ said each sub-module for conformance with timing requirements for ~~the individual sub-blocks~~ said each sub-module.

6. (Currently Amended) The method of claim 5, wherein the ~~gate-level netlists are~~ netlist is generated for the said each sub-modules only if the timing requirements for ~~the individual sub-modules~~ said gate level design of said each sub-module are met.

7. (Currently Amended) The method of claim 6, wherein the step of synthesizing is re-performed and the ~~gate-level designs are~~ gate level design of said each sub-module is re-tested in an iterative manner to verify conformance of the ~~gate-level designs~~ gate level design with the timing requirements of ~~the individual sub-modules~~ said each sub-module.

8. (Original) The method of claim 7, wherein the step of synthesizing is further based on wire loads and input/output loads/drivers.

9. (Currently Amended) The method of claim 8, on wherein the step of ~~verifying for~~ conformance of the gate-level designs testing the gate level design of said each sub-module for conformance with design requirements of said each sub-module includes performing a dynamic ~~simulations~~ simulation on the ~~gate-level designs~~ gate level design of said each sub-module.

10. (Currently Amended) A method of synthesizing a register transfer level (RTL) based design of a system comprising the steps of:

determining sub-modules of a top level system;

determining individual time budgets for each sub-module based on timing requirements of the top-level system;

synthesizing ~~gate-level designs~~ a gate level design of the said each sub-module based on the determined time budgets for ~~the individual sub-modules~~ said each sub-module;

generating a netlist for the gate level design of said each sub-module;

integrating the ~~gate-level designs netlist~~ of ~~the individual sub-modules~~ said each sub-module to form a an integrated top level design netlist;

testing the integrated top-level design netlist for conformance with top-level design requirements; and

~~generating gate-level netlists for the gate-level designs of each of the sub-modules; and~~

generating a top-level netlist when the integrated top-level design netlist conforms to the top-level design requirements.

Claim 11 (Cancelled)

12. (Currently Amended) The method of claim ~~11~~ 10, further comprising testing the ~~gate-level designs~~ gate level design of said each sub-module for conformance with ~~gate-level~~ design requirements of ~~the individual sub-modules~~ said each sub-module prior to integrating the ~~gate-level designs netlists~~ to form the integrated top-level design netlist.

13. (Currently Amended) The method of claim 12, wherein testing the ~~gate-level designs include~~ gate level design of said each sub-module includes performing static timing analysis on ~~the individual sub-modules~~ said each sub-module for conformance with timing requirements for ~~the individual sub-blocks~~ said each sub-module.

14. (Currently Amended) The method of claim 13, wherein the ~~gate-level netlists are~~ netlist for the gate level design of said each sub-module is generated for ~~the sub-modules~~ only if the timing requirements for ~~the individual sub-modules~~ said each sub-module are met.

15. (Currently Amended) The method of claim 14, wherein the step of synthesizing is re-performed and the ~~gate-level designs are~~ gate level design is re-tested in an iterative manner for verifying conformance of the ~~gate-level designs~~ gate level design with the timing requirements of ~~the individual sub-modules~~ said each sub-module.

16. (Currently Amended) The method of claim 15, wherein the step of synthesizing ~~gate-level designs~~ a gate level design is further based on wire loads and input/output loads/drivers.

17. (Currently Amended) The method of claim 16, wherein the step of ~~verifying~~ testing the gate level design of said each sub-module for conformance ~~of the gate-level designs with~~ design requirements includes performing ~~a dynamic simulations~~ simulation on the ~~gate-level designs~~ gate level design of said each sub-module.